IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **ALIA ET AL.**

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **POWER DOWN PROTOCOL FOR INTEGRATED CIRCUITS**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL747059609US

DATE OF DEPOSIT: November 5, 2001

NAME: Jennifer Ferguson

SIGNATURE: Jennifer Ferguson

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label FIGS. 1-3 as prior art. FIGS. 2, 3, 4 and 10 are being modified to remove extraneous markings therefrom as indicated in red ink. FIGS. 6 and 8 are also being modified to include a box as indicated in red ink around the flow diagram.

In the Specification:

Please replace the paragraph beginning at page 5, lines 26-28, with the following rewritten paragraph:

-- One aspect of the invention is directed to a system-on-chip (SOC) comprising a plurality of circuit blocks,

each responsive to a respective local clock signal. A system clock is connected to the circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals.

A power control manager is connected to the circuit blocks for selectively providing a shutdown signal thereto. Each circuit block comprises a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block provides a shutdown acknowledgment signal to the power control manager. --

Please replace the paragraph beginning at page 5, lines 28-31, with the following rewritten paragraph:

-- Another aspect of the invention is directed to a method for powering down circuit blocks within a system-on-chip (SOC) comprising a plurality of circuit blocks. The method comprises providing a system clock signal to the circuit blocks for functioning as a respective local clock signal, selectively providing a shutdown signal to the circuit blocks, and preventing the system clock signal from functioning as the local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment signal. --

In the Claims::

Please cancel Claims 1 to 11.

Please add new Claims 12 to 38.

12. A system-on-chip (SOC) comprising:

a plurality of circuit blocks, each responsive to a respective local clock signal;

a system clock connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals;

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto; and

each circuit block comprising a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment signal to said power control manager.

13. An SOC according to Claim 12, wherein each shutdown circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

14. An SOC according to Claim 12, wherein said power control manager is connected to each shutdown circuit through a respective power down request line for providing the shutdown signal thereto, and through a respective power down acknowledgment line for receiving the shutdown acknowledgment signal therefrom.

15. An SOC according to Claim 14, wherein each circuit block further comprises a block logic circuit

connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

16. An SOC according to Claim 14, wherein each shutdown circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to said system clock, and an output for providing the respective local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

17. An SOC according to Claim 14, wherein said power control manager comprises:

a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals; and

a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals.

18. An SOC according to Claim 17, further comprising a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said first and second registers.

19. An SOC according to Claim 12, further comprising another system clock connected to selected circuit blocks for providing a system clock signal thereto.

20. A system-on-chip (SOC) comprising:

a plurality of circuit blocks;

a system clock connected to said circuit blocks for providing a system clock signal thereto; and

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto; and

each circuit block comprising

a block logic circuit having an input for receiving the shutdown signal, and an output for providing a shutdown acknowledgment signal to said power control manager after receiving the shutdown signal, and

a shutdown circuit connected to said block logic circuit for preventing the system clock signal from functioning as a local clock signal after said block logic circuit provides the shutdown acknowledgment signal to said power control manager.

21. An SOC according to Claim 20, wherein each shutdown circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

22. An SOC according to Claim 20, wherein said power

control manager is connected to each shutdown circuit through a respective power down request line for providing the shutdown signal thereto, and through a respective power down acknowledgment line for receiving the shutdown acknowledgment signal therefrom.

23. An SOC according to Claim 22, wherein each block logic circuit is connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

24. An SOC according to Claim 22, wherein each shutdown circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to said system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

25. An SOC according to Claim 22, wherein said power control manager comprises:

a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals; and

a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals.

26. An SOC according to Claim 25, further comprising a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said first and second registers.

27. A system-on-chip (SOC) comprising:

a plurality of circuit blocks;

a system clock connected to said circuit blocks for providing a system clock signal thereto;

a power control manager connected to said circuit blocks through a respective power down request line for selectively providing a shutdown signal thereto, and through a respective power down acknowledgment line for receiving a shutdown acknowledgment signal therefrom, said power control manager comprising at least one register for storing data indicating logic states of the shutdown signals and the shutdown acknowledgment signals;

a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said at least one register; and

each circuit block comprising a shutdown circuit for preventing the system clock signal from functioning as a local clock signal after the circuit block receiving the shutdown signal provides the shutdown acknowledgment signal to said power control manager.

28. An SOC according to Claim 27, wherein each shutdown circuit comprises a clock separation circuit connected to said power control manager for preventing the

system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

29. An SOC according to Claim 27, wherein each circuit block further comprises a block logic circuit connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

30. An SOC according to Claim 28, wherein each clock separation circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to said system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

31. An SOC according to Claim 27, wherein said at least one register comprises:

a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals; and

a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals.

32. A method for powering down circuit blocks within

a system-on-chip (SOC) comprising a plurality of circuit blocks, the method comprising:

providing a system clock signal to the circuit blocks for functioning as a respective local clock signal;

selectively providing a shutdown signal to the circuit blocks; and

preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment signal.

33. A method according to Claim 32, further comprising preventing the system clock signal from functioning as the respective local clock signal if the corresponding circuit block receiving the shutdown signal is in an idle state.

34. A method according to Claim 32, wherein the SOC comprises a power control manager for providing the shutdown signals, and wherein each circuit block comprises a shutdown circuit connected to the power control manager through a respective power down request line for receiving the shutdown signal therefrom, and through a respective power down acknowledgment line for providing the shutdown acknowledgment signal thereto.

35. A method according to Claim 34, wherein each circuit block further comprises a block logic circuit connected to the shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgment line for

providing the shutdown acknowledgment signal thereto.

36. A method according to Claim 34, wherein each shutdown circuit comprises a logic circuit having a first input connected to the respective power down request line, a second input connected to the respective power down acknowledgment line, and a third input connected to a system clock, and an output for providing the respective local clock signal based upon logic states of the shutdown signal, the shutdown acknowledgment signal and the system clock signal.

37. A method according to Claim 34, wherein the power control manager comprises a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals, and a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals.

38. A method according to Claim 37, further comprising determining whether each circuit block is in an active state or an idle state by querying the first and second registers.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the

statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below. Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached paper is captioned "Version With Markings to Show Changes Made."

Respectfully submitted,

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In re Patent Application of:
ALIA ET AL.
Serial No. **Not yet assigned**
Filing Date: **Herewith**
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at page 5, line 26-28 has been amended as follows:

[Based on this idea, this invention provides a selective power down circuit as previously indicated and defined in the characterizing portion of Claim 1.] One aspect of the invention is directed to a system-on-chip (SOC) comprising a plurality of circuit blocks, each responsive to a respective local clock signal. A system clock is connected to the circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals.

A power control manager is connected to the circuit blocks for selectively providing a shutdown signal thereto. Each circuit block comprises a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block provides a shutdown acknowledgment signal to the power control manager.

Paragraph beginning at page 5, line 28-31 has been amended as follows:

[Additionally, this invention provides a method for powering down individual circuit blocks within a system-on-chip as previously indicated and defined in the characterizing portion of Claim 7.] Another aspect of the invention is directed to a method for powering down circuit blocks within a system-on-chip (SOC) comprising a plurality of circuit blocks.

The method comprises providing a system clock signal to the circuit blocks for functioning as a respective local clock signal, selectively providing a shutdown signal to the circuit blocks, and preventing the system clock signal from functioning as the local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgment signal.

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EXPRESS MAIL NO: EL747059609US

DATE OF DEPOSIT: November 5, 2001

NAME: Jennifer Ferguson

SIGNATURE: Jennifer Ferguson

SUBMISSION OF PROPOSED MODIFICATIONS TO DRAWINGS

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label FIGS. 1-3 as prior art. FIGS. 2, 3, 4 and 10 are being modified to remove extraneous markings therefrom as indicated in red ink. FIGS. 6 and 8 are also being modified to include a box as indicated in red ink around the flow diagram.

Respectfully submitted,

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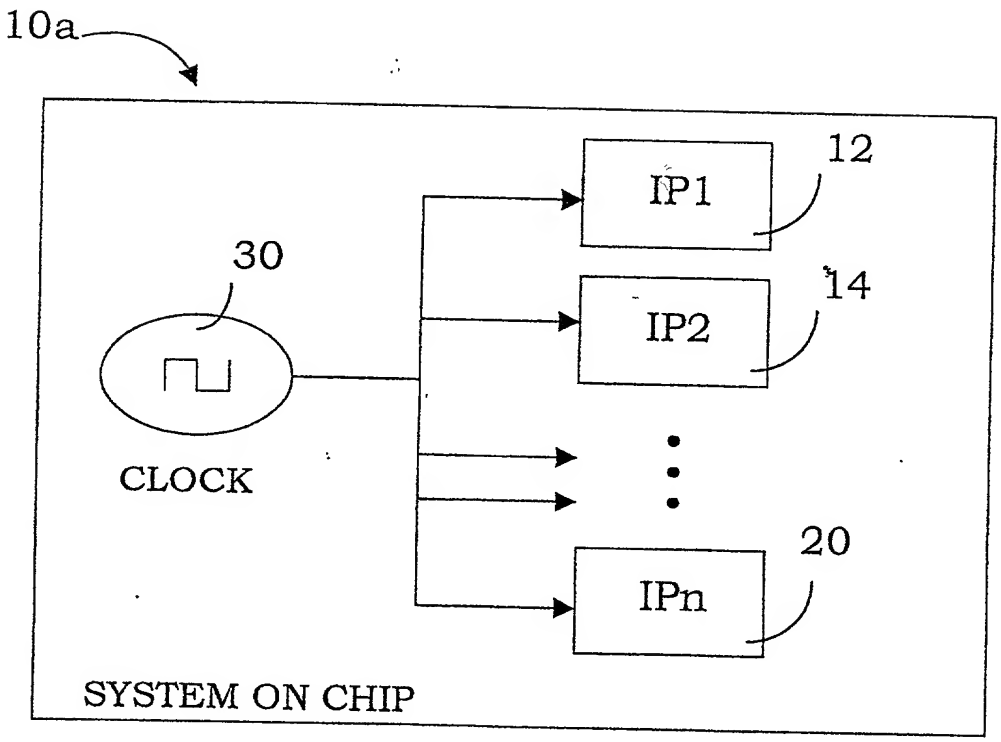

FIG. 1
(PRIOR ART)

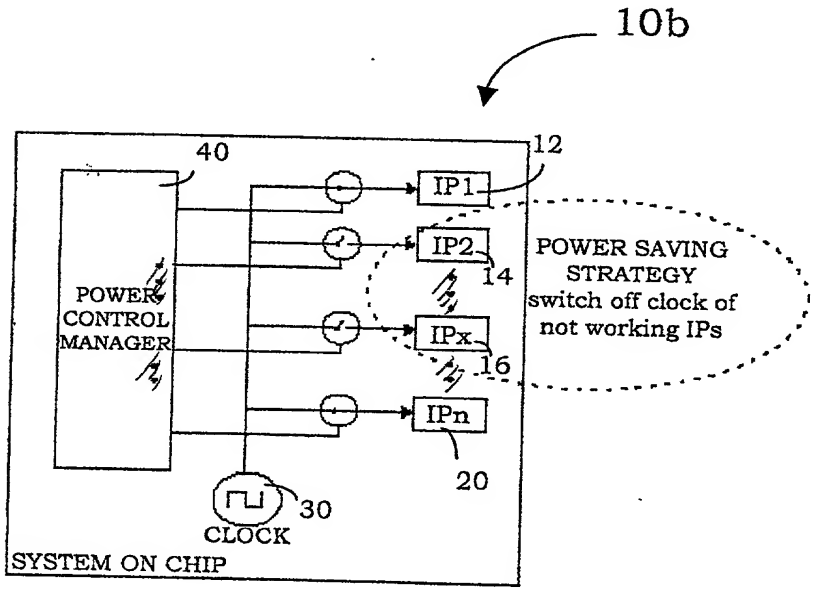

FIG. 2
(PRIOR ART)

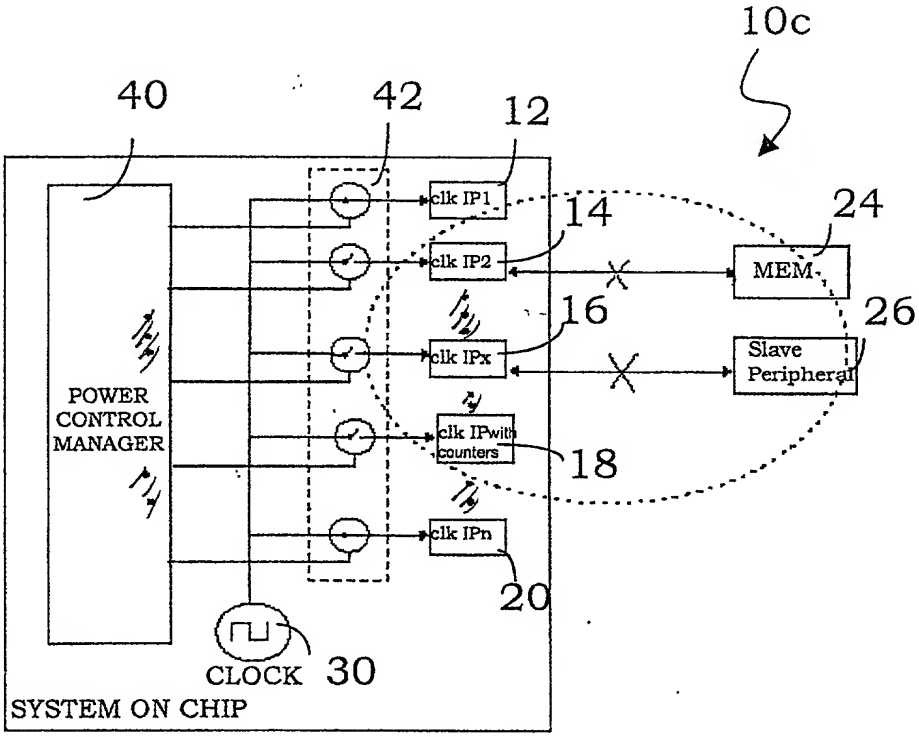

FIG. 3
(PRIOR ART)

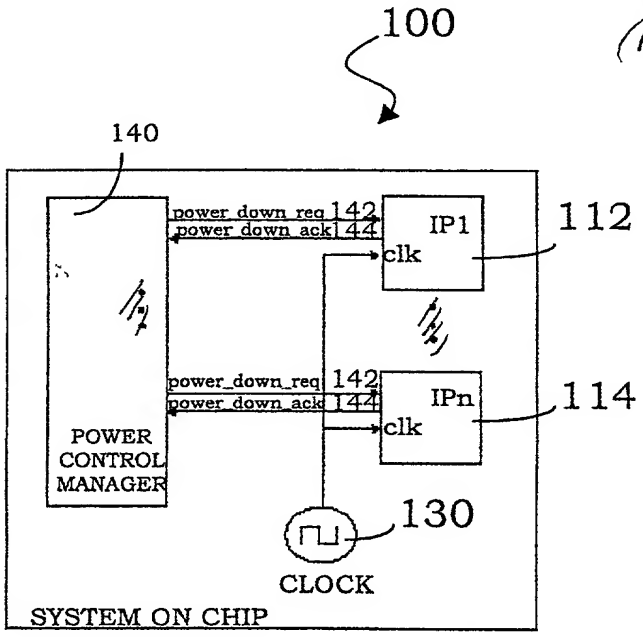

FIG. 4

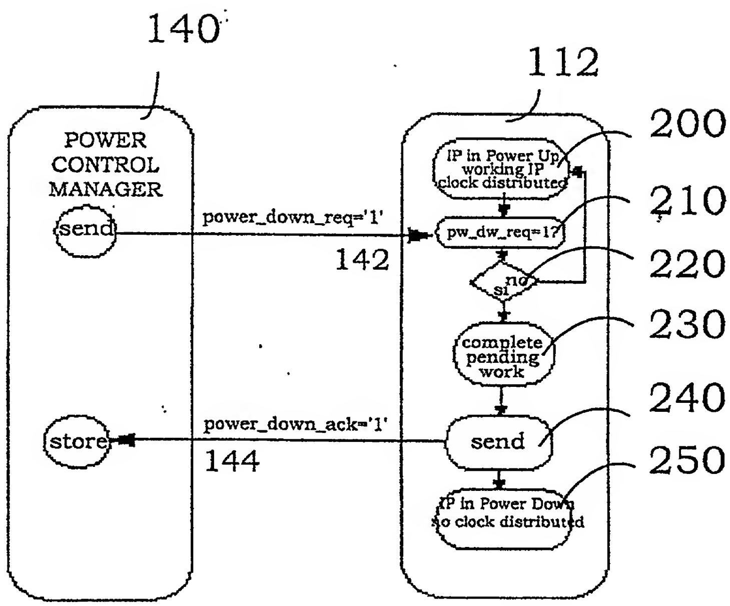

FIG. 5

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Power Down Manager:
        sent to the IP the power_down_req signal set to '1';

IP:
        IF power_down_req is asserted (='1'):
                    complete its pending work;
                    set power_down_ack to '1';
                    stop its own clock => IP halted;
        else
                    normal work;

Power Down Manager:
        Stores the value of power_down_ack to allow visibility
        of IP status (power on/off);
```

FIG. 6

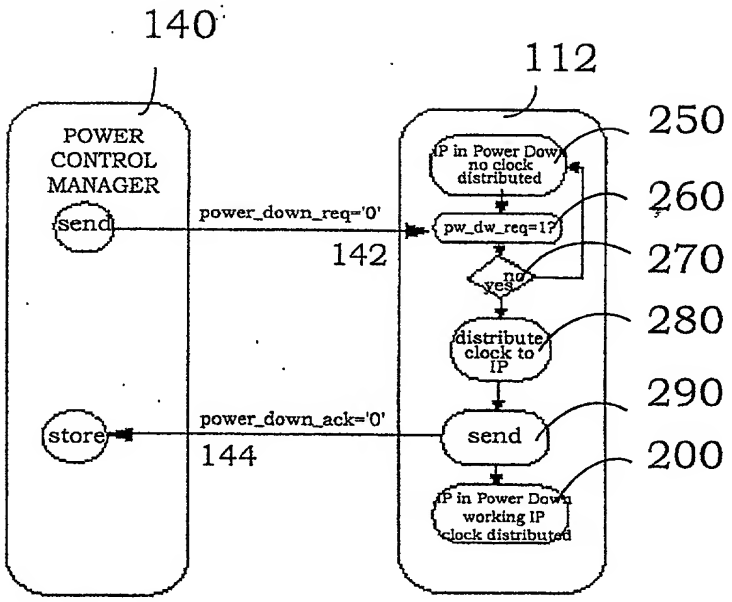

FIG. 7

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Power Down Manager:
        sent to the IP the power_down_req signal set to '0';

IP:
        IF power_down_req is de_asserted (='0'):
                    restarts its own clock;
                    set power_down_ack = '0';
                    restart to work;
        else
                    no clock distributed to IP => IP halted;

Power Down Manager:
        Stores the value of power_down_ack to allow visibility
        of IP status (power on/off);
```

FIG. 8

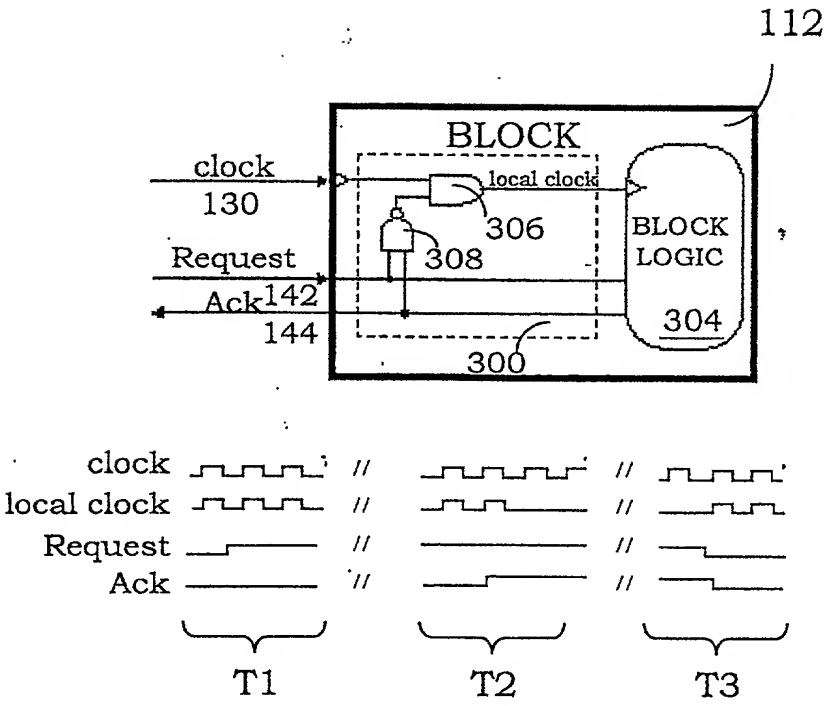
112
BLOCK
clock
130
local clock
306
308
Request
Ack
142
144
BLOCK
LOGIC
304
300
clock
local clock
Request
Ack
T1
T2
T3

FIG. 9

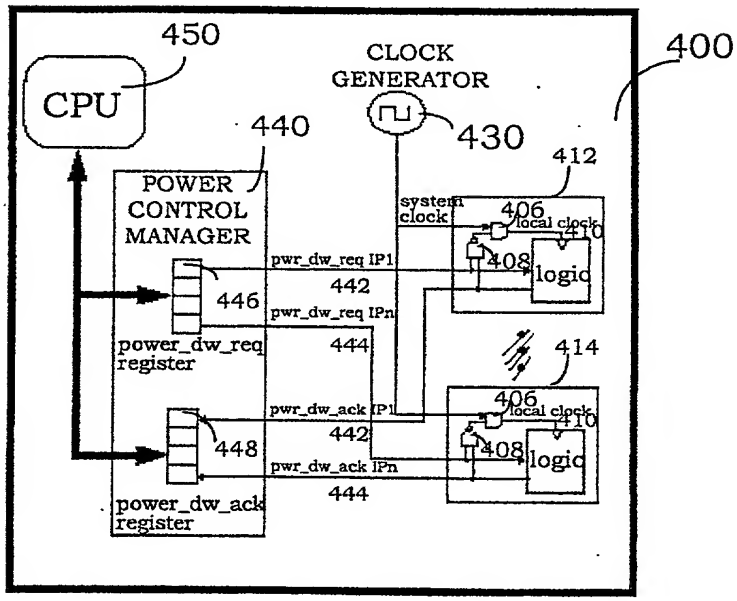
450
CPU
CLOCK
GENERATOR
400
440
430
412
POWER
CONTROL
MANAGER
system
clock
406
local clock
410
408
logic
pwr_dw_req IP1
442
446
pwr_dw_req IPn
power_dw_req
register
444
414
406
local clock
410
pwr_dw_ack IP1
442
448
408
logic
pwr_dw_ack IPn
444
power_dw_ack
register

FIG. 10